AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions of the claims and any prior listing of the claims in the present application. The status of each claim is shown in parentheses.

In the following listing, Claims 1-7, 9-17, 22, and 24-28 are canceled herein. Claims 8, 18–21 and 23 were previously cancelled. Claim 29 remains as previously presented and allowed.

Listing of Claims

Claims 1-28 **(Cancelled)**

Claim 29 **(Previously Presented)**: A disk drive controller comprising:

a buffer memory for storing write operation data;

a buffer memory controller comprising:

a data buffer configured to buffer write operation data between the buffer memory and a write head of a disk;

a plurality of address registers configured to store, for each of a plurality of write operations, an address identifying a location of corresponding write operation data stored within the buffer memory; and

controller logic configured to transfer, for each of the write operations, the corresponding write operation data from the buffer memory to the data buffer based at least upon the corresponding address stored in the address registers;

and

a microprocessor that issues commands to the controller logic, the microprocessor configured to perform write operations in an order other than the order in which the write operations are received by the buffer memory, wherein the microprocessor executes firmware code that causes the microprocessor to:

(A) identify a first write operation received by the buffer memory;

(B) identify a second write operation received by the buffer memory after receiving the first write operation;

(C) load a first of the address registers of the buffer memory controller with an address in the buffer memory of the write operation data of the second write operation;

(D) load a second of the address registers of the buffer memory controller with an address in the buffer memory of the write operation data of the first write operation; and

(E) issue a single command to the buffer memory controller that causes the buffer memory controller to transfer the data identified by the first address register and to subsequently transfer the data identified by the second address register.